MICROWAVE CHARACTERIZATION OF FLIP-CHIP MMIC INTERCONNECTIONS

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Abstract — **We report accurate on-wafer measurements of transmission lines on flip-chip coplanar-waveguide MMICs. The effects are difficult to predict theoretically, and, without custom standards and unique calibration software, measurements would be intractable. The results are applicable to the development of an accurate CAD database. We also report and apply a new technique for the measurement of transmission line capacitance.**

INTRODUCTION

Flip-chip mounting, a natural packaging technique for coplanar waveguide (CPW) components, has recently come into use [1,2,3]. This process has the potential for low-cost, high-yield, high-volume applications. However, one potential roadblock is the lack of accurate electrical data for use in computer-aided design (CAD). Specific problems include (1) the lack of validated CPW models for simple circuit components, (2) the absence of microwave descriptions of solder-ball joints and bridges, and (3) the unknown loading effect of the substrate, which is close to the processed side of the chip after flip mounting.

These issues can be addressed by accurate on-wafer measurements. These are useful not only in selecting the appropriate technologies but also in constructing a detailed and accurate database of electrical descriptions of the on-chip components, transmission lines, and interconnects which compose the circuit. The methods are not difficult to apply, and the resulting data can be used repeatedly in design, obviating the need for exhaustive, and sometimes unreliable, theoretical modeling.

Conventional wafer-probe calibrations make use of commercial artifact standards. Such "off-wafer" calibrations may be adequate in some cases but fail entirely in others [4]. Even for the modeling of transmission lines and simple passive circuit elements, commercial techniques imprecisely specify the reference plane and thereby introduce uncertainty into the model. Some packaging measurements are even less amenable to off-wafer calibration. For example the solder bump spacing of flip-chips such as those of [1] and [3] is over 450 μm. This far exceeds the pitch of commercial, lumped-element microwave probe calibration standards and makes calibrations based on such standards highly unreliable when applied to on-substrate measurements. Furthermore, off-wafer calibrations are not readily applicable to the characterization of solder ball joints or other transitions between different transmission line configurations.

In this paper, we report measurements obtained using custom, on-wafer standards along with the calibration software MultiCal, which implements the multiline TRL (through-reflect-line) calibration [5] with correction for nonideal characteristic impedance [6,7]. This method, which provides precisely defined measurement reference planes and reference impedance, has been used as a benchmark for determining the accuracy of commercial on-wafer calibrations [8]. It is applicable to the characterization of passive on-chip components, such as MIM capacitors and spiral inductors [9]. Here we use the method to characterize on-chip transmission lines and determine their lumped-element equivalent circuits.

TEST STRUCTURES

We fabricated coplanar waveguide TRL calibration structures using technology similar to that of [1] and [3]. The coplanar lines, on 625 μm GaAs, consisted two consecutive layers of evaporated Ti/Au followed by 3 μm of gold plating. The center conductor and gap widths were each 50 μm and the ground planes were approximately 440 μm wide. In some cases, a 0.1 μm layer of Si_3N_4 was deposited on the GaAs before metallization. Some of the wafers were passivated with 2 μm of SiO_2 before plating. This oxide layer, used to support bridges interconnecting the CPW ground planes, spiral inductors, etc., was etched from the transmission lines before plating. A second SiO_2 passivation layer was added as a final step. Table 1 lists the properties of the lines whose measurements are reported here. In each of these cases, we built two nominally-identical lines of length 1.0 mm and 5.8 mm.

CALIBRATION AND MEASUREMENT

We characterized the TRL calibration structures using a frequency-domain network analyzer and on-wafer probes. We used the multiline TRL calibration [5], which provides *S*-parameters normalized to the characteristic impedance Z_o of the line and which also provides the propagation constant and loss of the line. In order to determine impedance parameters and transmission line equivalent circuit parameters, we determined Z_o using the method of [6]. This method requires a knowledge of C_{dc}, the dc capacitance per unit length of the line. This we measured by a modified version of the "direct comparison method" of [7]. In this case, we first calibrated using a well-characterized set of NIST-built CPW standard lines. We then performed a second-tier multiline TRL calibration using the unknown lines and analyzed the resulting calibration error coefficient to estimate Z_o of the unknown lines at each frequency [10,11]. Using the known relationship between Z_o, C, and the propa-

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gation constant [5], we were able to estimate C at each frequency (Fig. 1). We averaged the low-frequency values from 0.25 to 2.5 GHz to determine C_{dc}.

Transmission Line Parameters

Figure 2 shows the real part of the measured effective relative permittivity $\varepsilon_{r,eff}$. We expect differences between the curves due to differences in dielectric passivation layers. However, since lines B and H are nominally identical, the difference between those curves must be due to processing variations. Also shown is data from a published CPW model [12], applicable only to lines B and H. At frequencies at which the skin depth is large compared to the metal thickness, $\mathrm{Re}(\varepsilon_{r,eff})$ is significantly less than the customary prediction of approximately 7.0, which is based on the assumption of perfectly conducting, thin metal. Analysis using the model demonstrates that finite conductor thickness causes this drop by depressing L.

Figure 3 shows that the measured loss is nearly independent of the deposited dielectrics. In particular, there is little evidence of a significant effect of the nitride.

Figure 4 displays the real part of the characteristic impedance Z_o and shows that, for line B, the model demonstrates the primary features. Figure 5 shows that the variations in $\mathrm{Im}(Z_o)$ among the various lines are small.

Figures 6 and 7 show measurements of the inductance L and resistance R (both per unit length). Predictions from the model are included. Even though the model does not account for the additional dielectric layers in lines A, D, and F, we have applied it to these cases for the computation of L and R since these parameters are virtually independent of the dielectrics in the quasi-TEM approximation. In order to reach the good agreement shown in the curves, we postulated that the metallization varied in both thickness and conductivity from wafer to wafer. The parameters used in the model are given in Table 1. Table 1 also shows a significant difference between three measured dc resistances R_{dc}, including those of the nominally identical wafers B and H.

In each of Figures 2–6, the accuracy apparently declines near multiples of 10 GHz. This is due to a slight, second-order, error when the transmission line length is a multiple of half a guide wavelength.

Conclusions

With its potential for low cost and high reliability, the flip-chip CPW MMIC holds promise for large-scale introduction into consumer electronics. Design of such circuits, however, is hampered by the lack of reliable electrical data on circuit elements. Such data are difficult to obtain theoretically. On the other hand, carefully designed and conducted measurements can provide accurate data, with well-defined reference planes, that can readily be integrated into a CAD database for high-quality, first-pass circuit design. We have presented data on transmission line parameters. We have also studied the characterization of on-chip components [9]. In order to characterize solder joint and loading effects, we have built an additional set of TRL calibration structures on the ceramic mounting substrate. However, the characterization of these structures using a two-tier calibration is not yet complete.

Acknowledgements

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Line Label	Nitride Layer (μm)	First Oxide (μm)	Second Oxide (μm)	Measured R_{dc} (Ω/cm)	Measured C_{dc} (pF/cm)	Modeled Metal Thickness (μm)	Modeled Conductivity (S/m)	Modeled GaAs Permittvity
A	0.1	2	2	0.89	1.72	8	$3.10 \cdot 10^7$	–
B	0	0	0	1.23	1.62	5	$3.30 \cdot 10^7$	13.125
D	0	2	1	–	1.69	7	$3.10 \cdot 10^7$	–
F	0	2	0.5	–	1.68	8	$2.95 \cdot 10^7$	–
H	0	0	0	1.31	–	–	–	–

Table 1: Transmission Line Properties

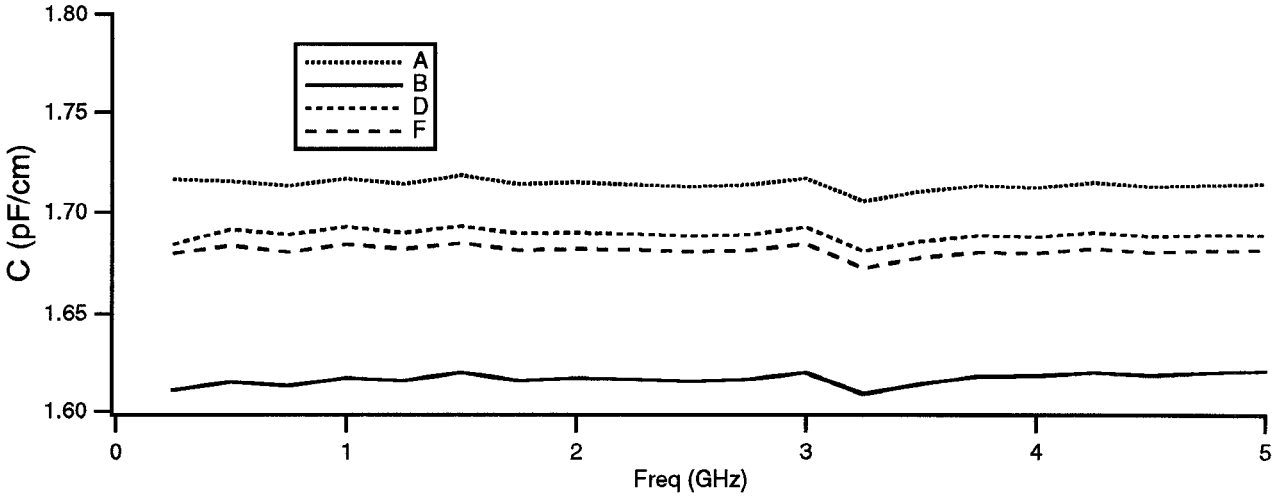

Figure 1: Capacitance per Unit Length

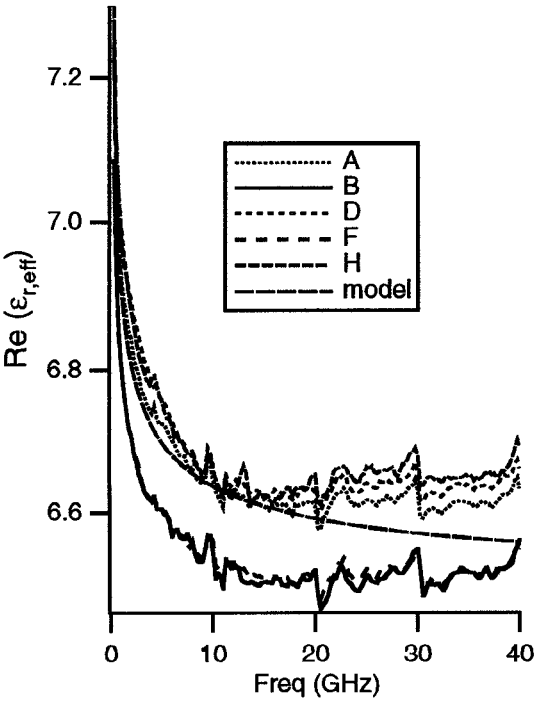

Figure 2: Effective Relative Permittivity

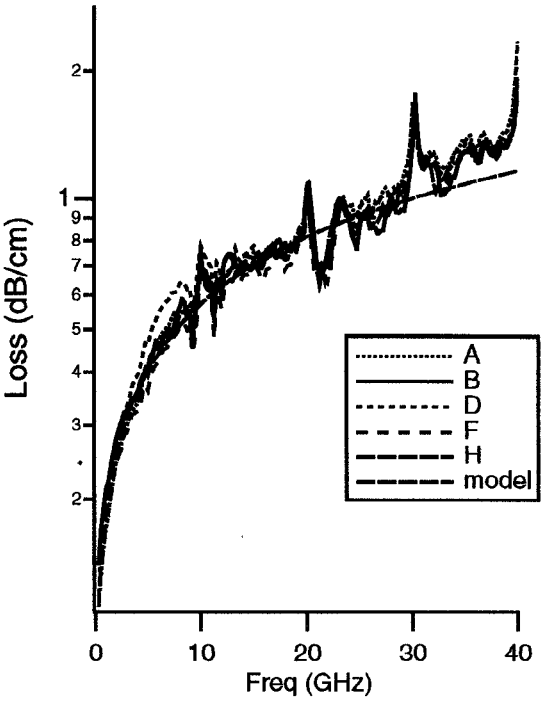

Figure 3: Attenuation

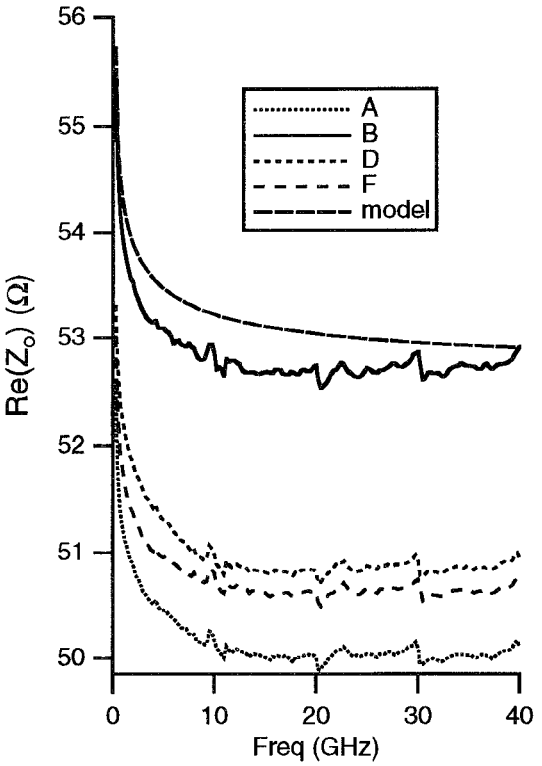

Figure 4: Characteristic Impedance, Real Part

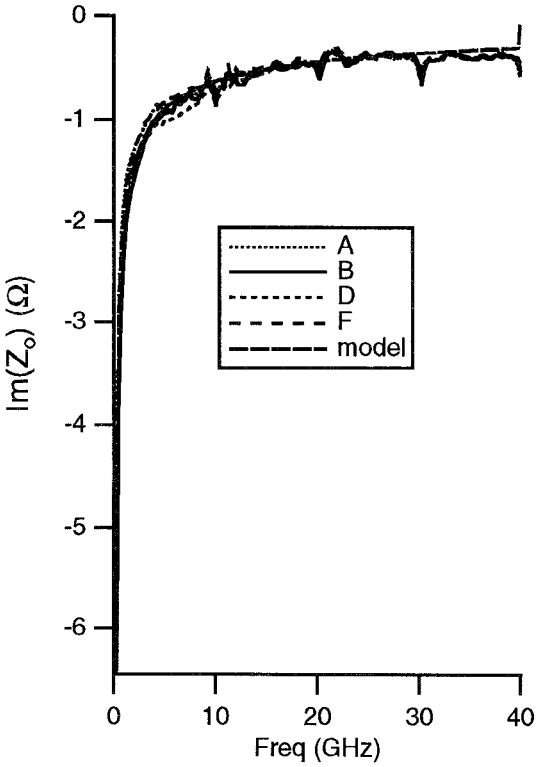

Figure 5: Characteristic Impedance, Imaginary Part

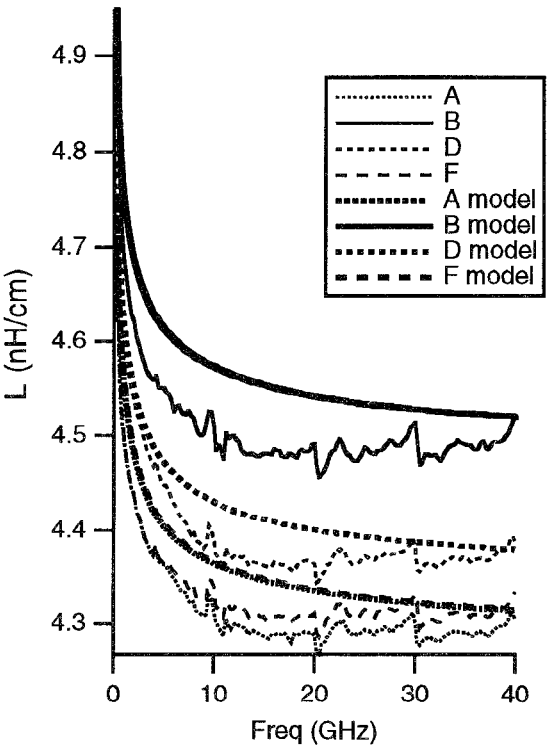

Figure 6: Inductance per Unit Length

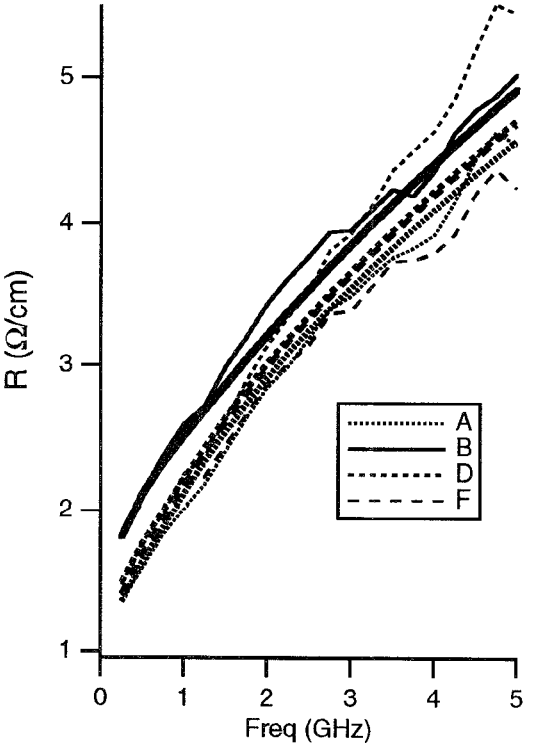

Figure 7: Resistance per Unit Length